

FIG. 1

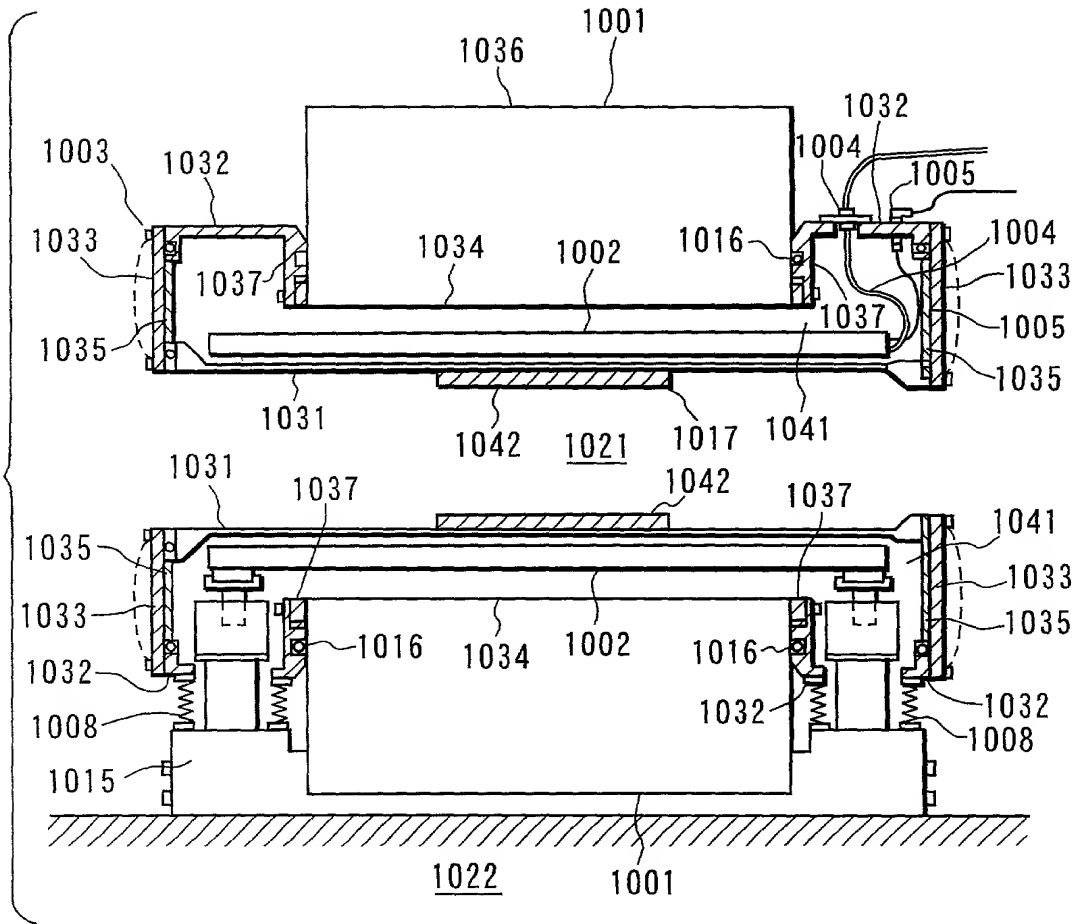


FIG. 2

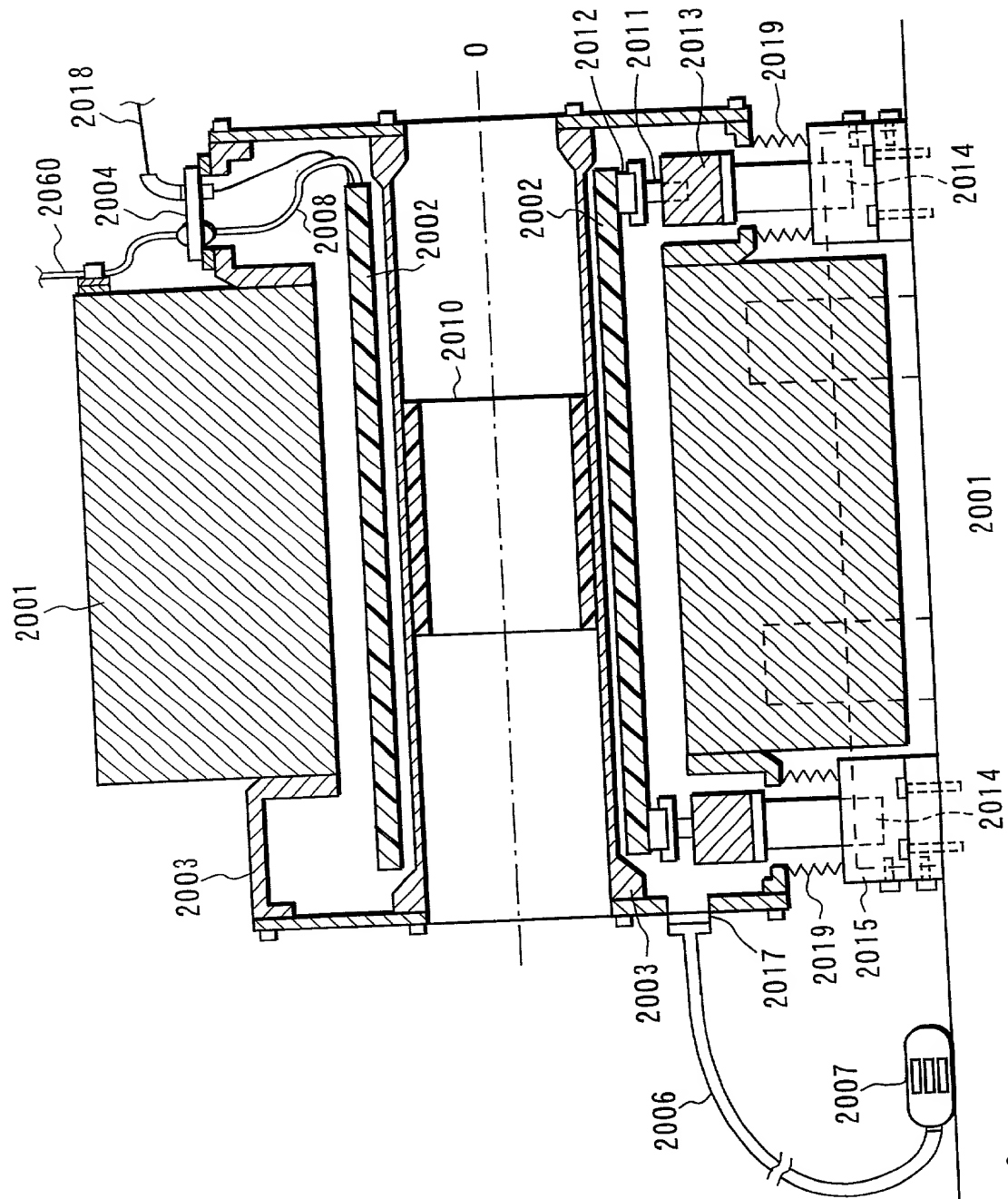


FIG. 3

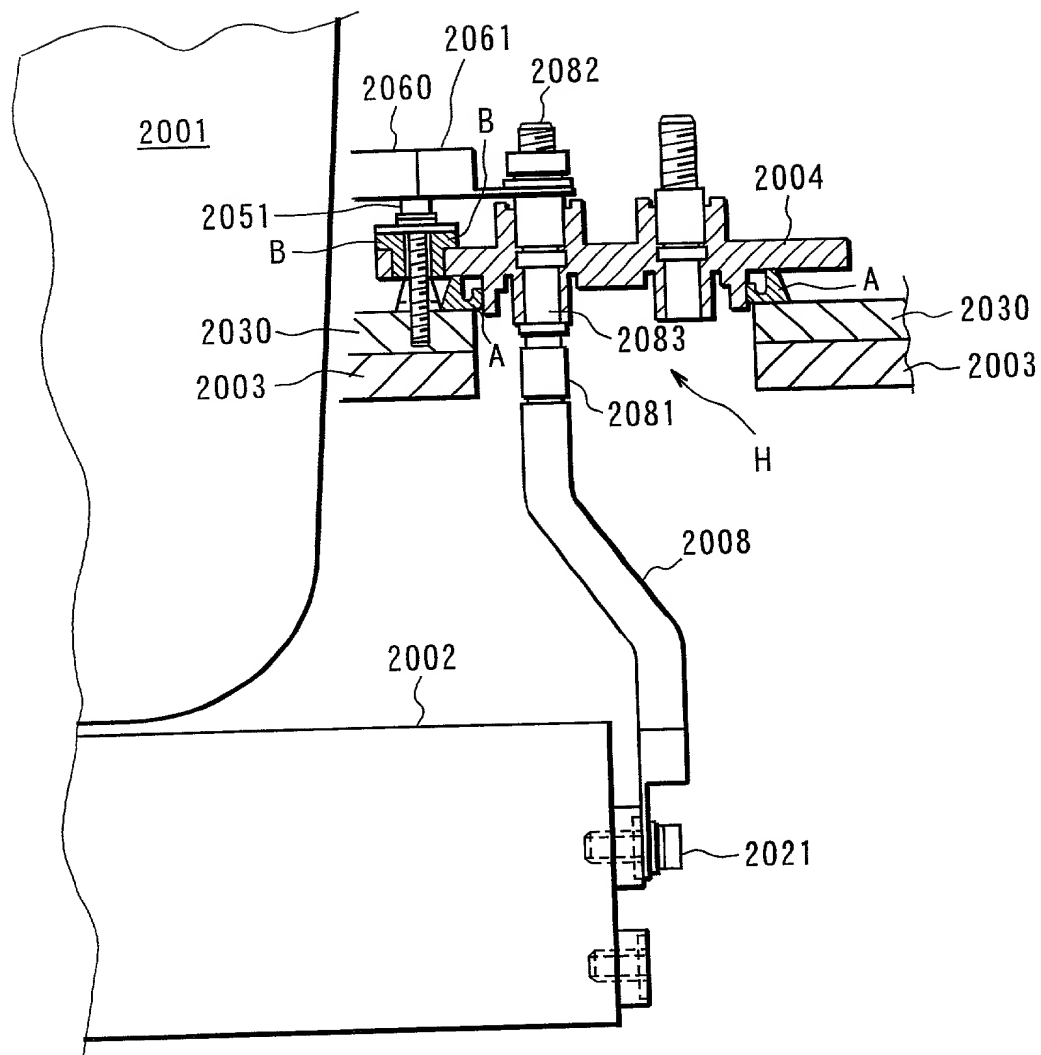


FIG. 4

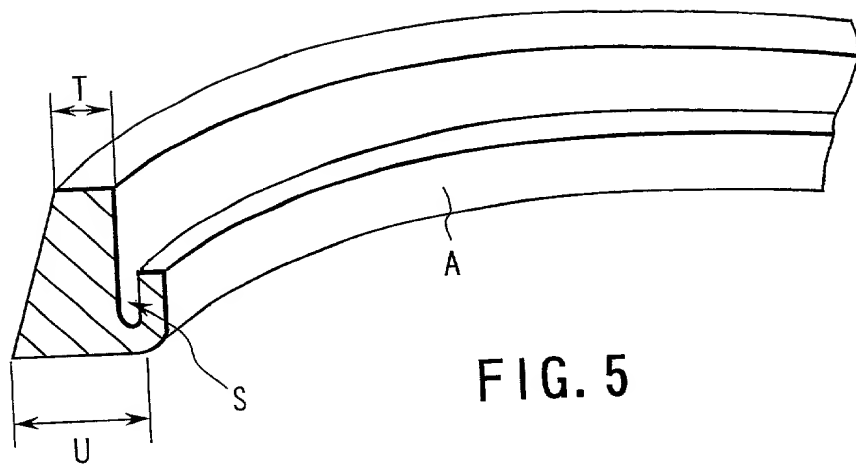


FIG. 5

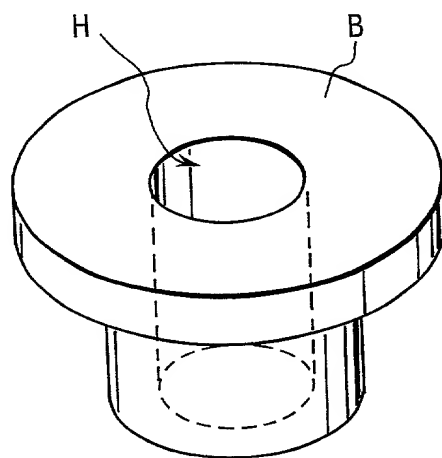


FIG. 6

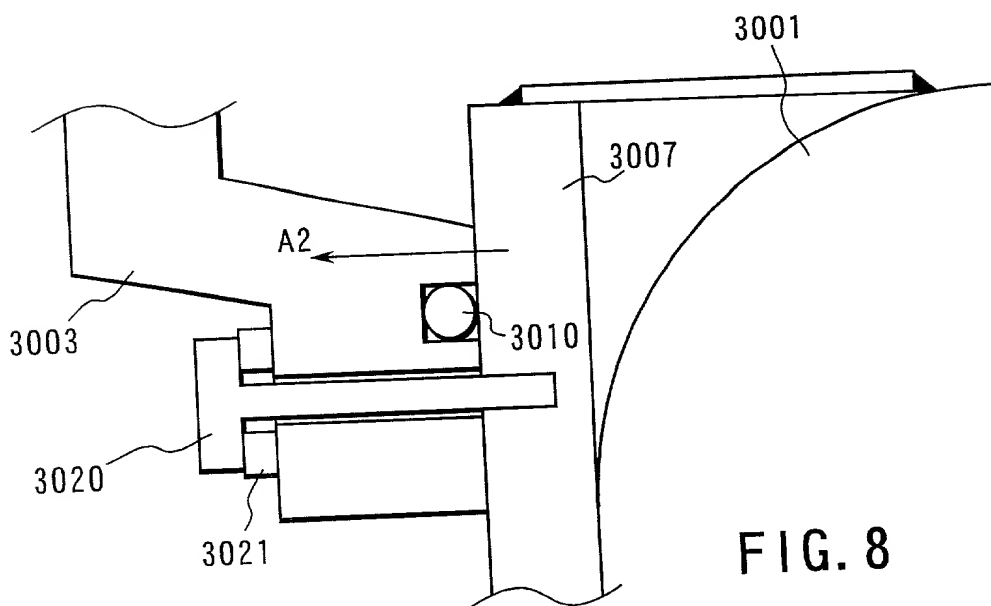


FIG. 8

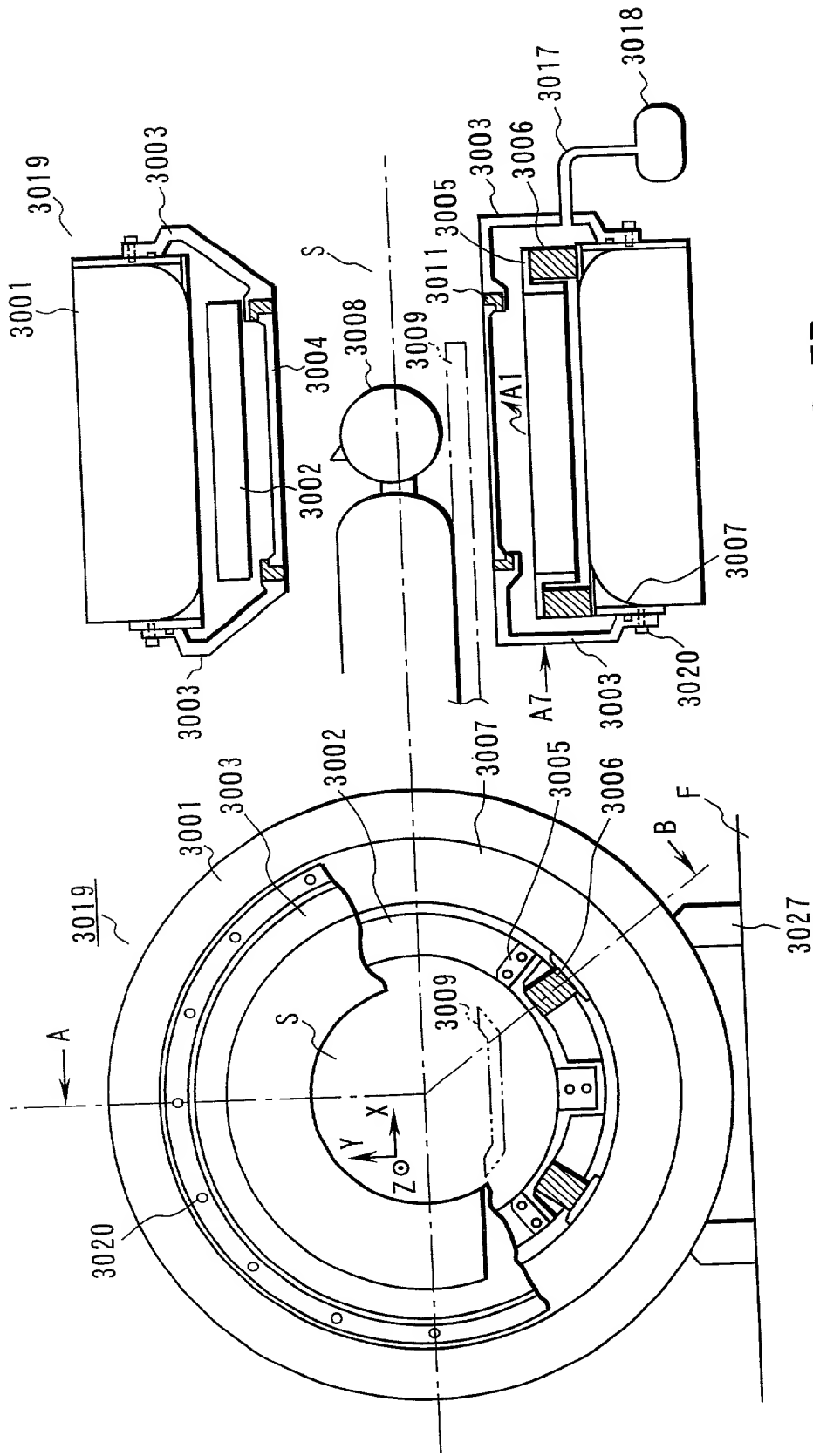
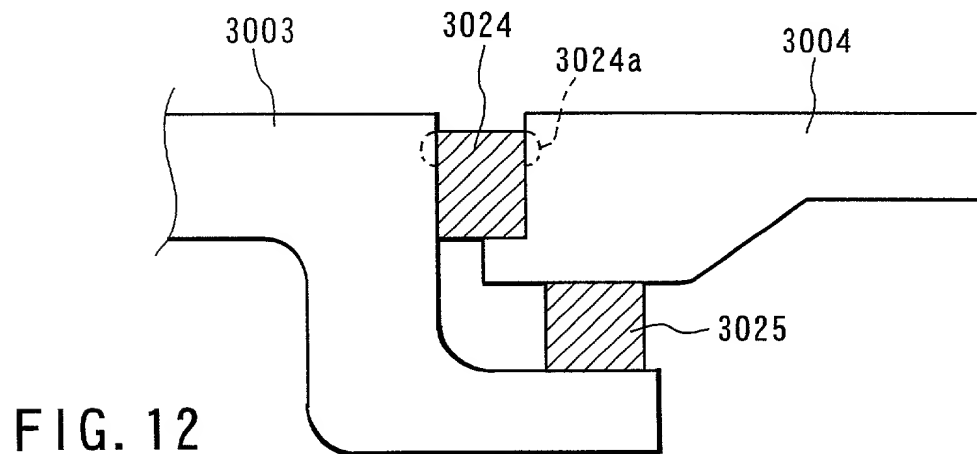
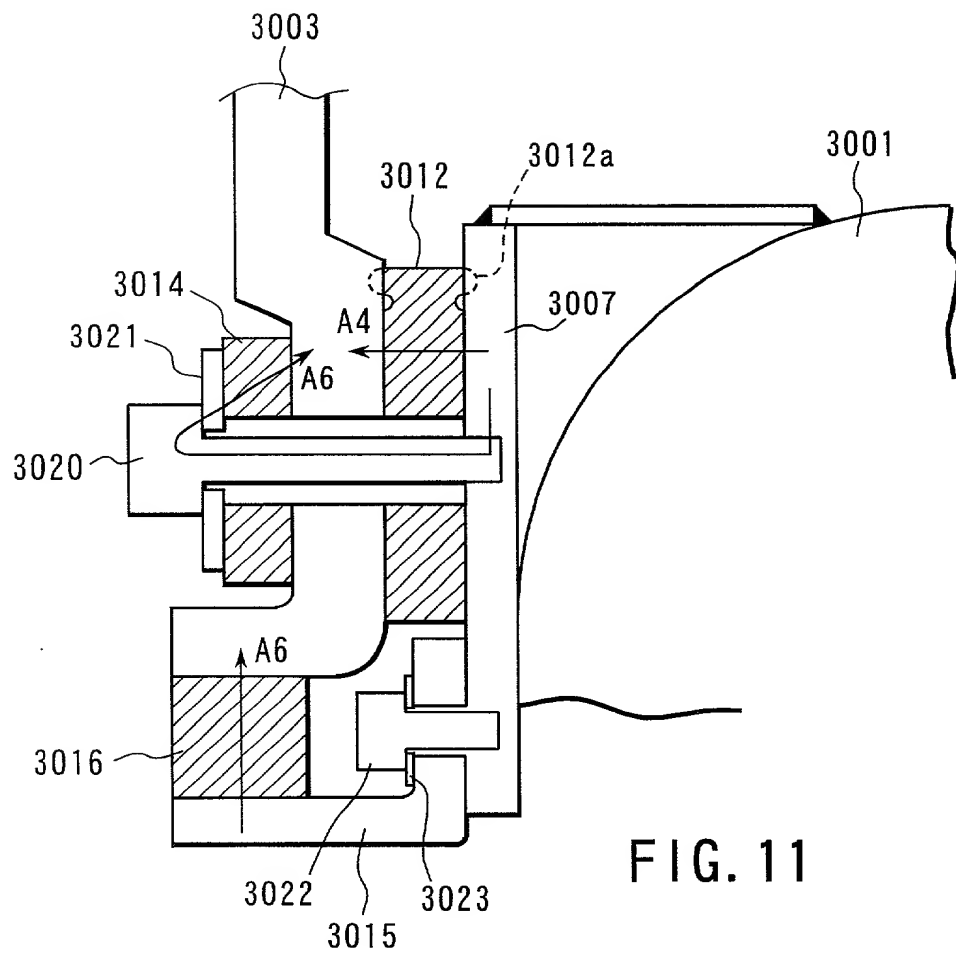


FIG. 7B

FIG. 7A

This cross-sectional view shows a gate stack (3003) on a substrate (3001). The gate stack includes a gate dielectric (3012) and a gate electrode (3012a). A source/drain region (3014) is formed in the substrate, containing a dopant (3021) and a conductive layer (3020). The gate stack is positioned over the source/drain region. Arrows A4 and A5 indicate the direction of the electric field or current flow.

FIG. 10



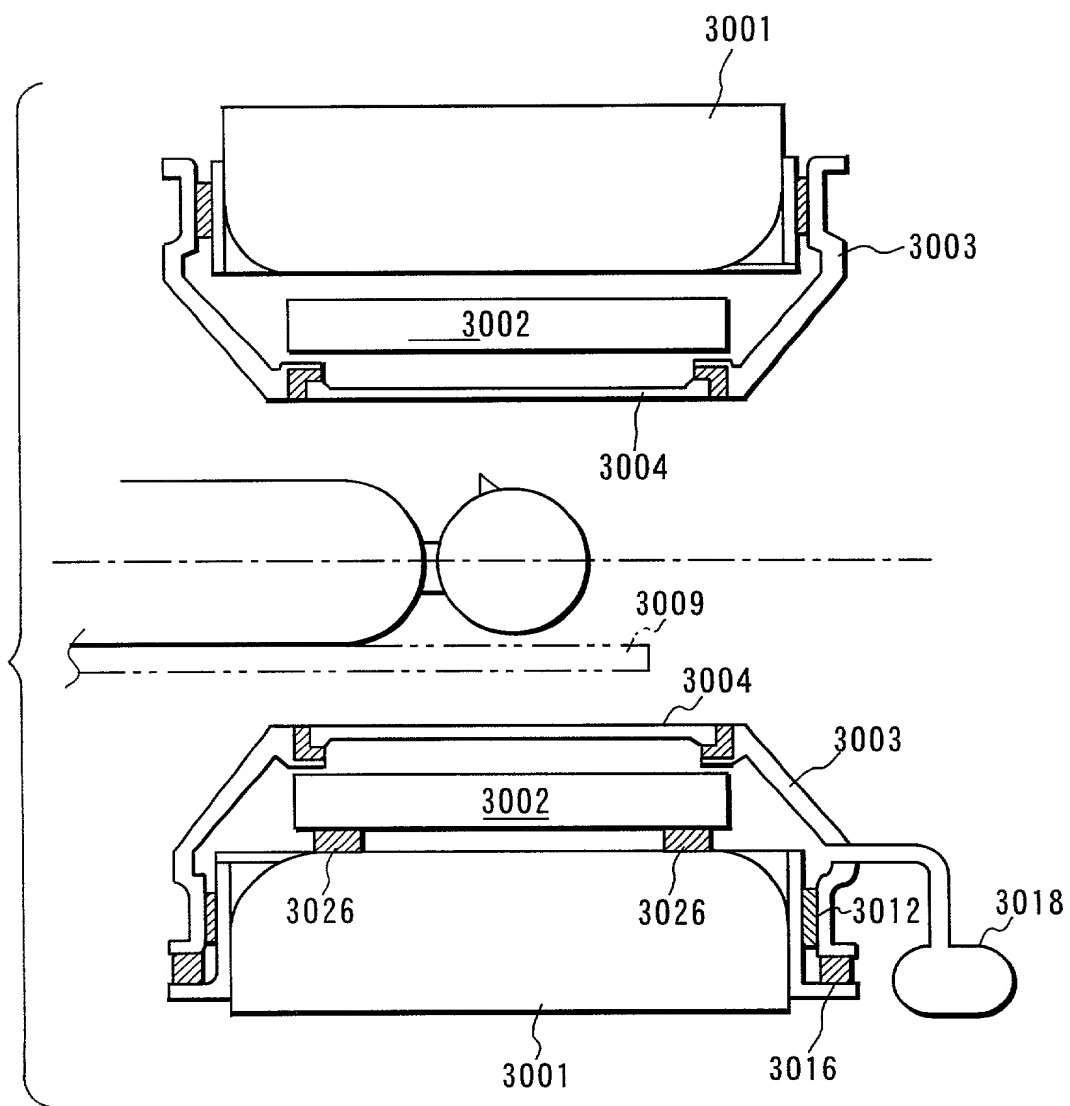


FIG. 13

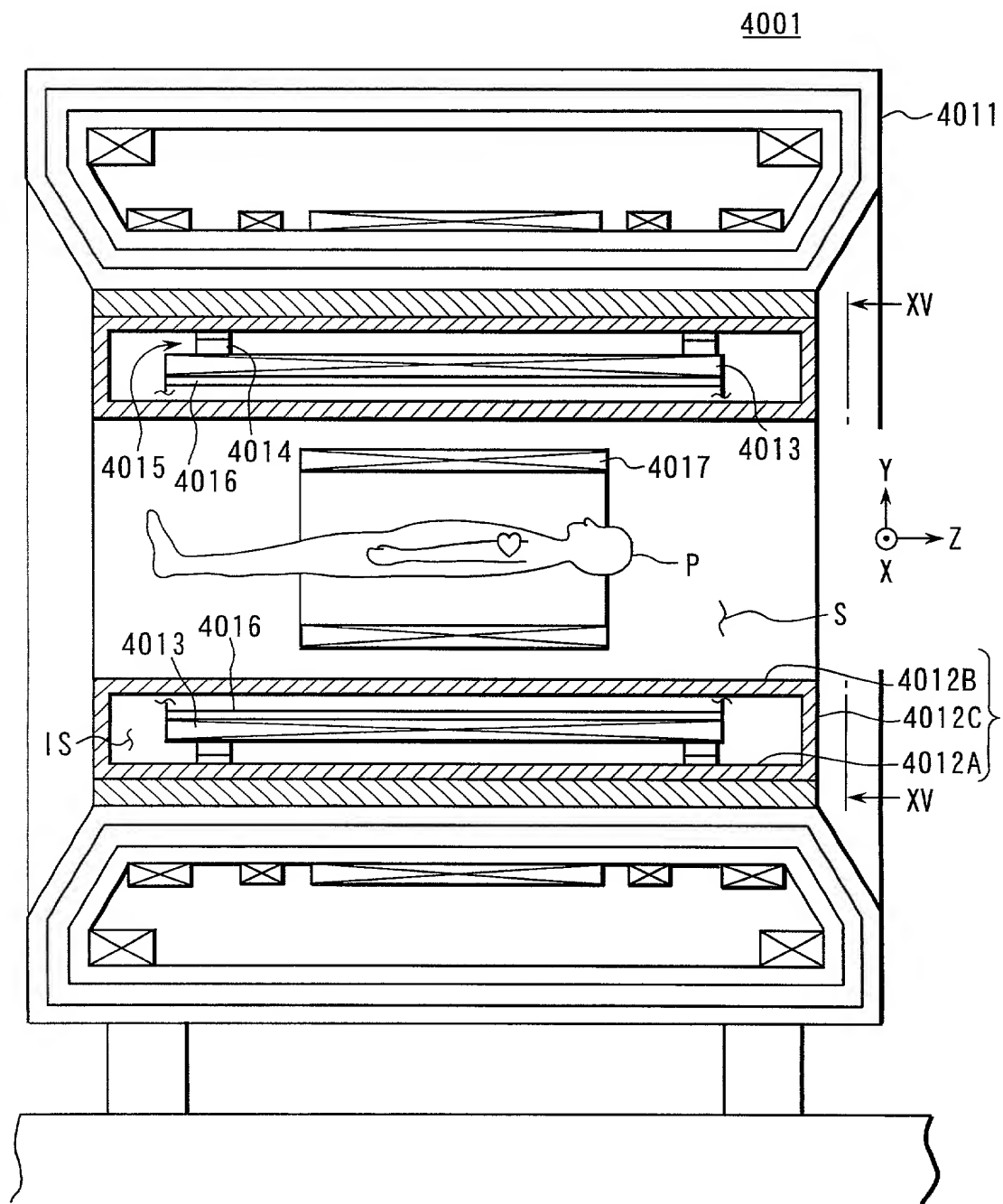
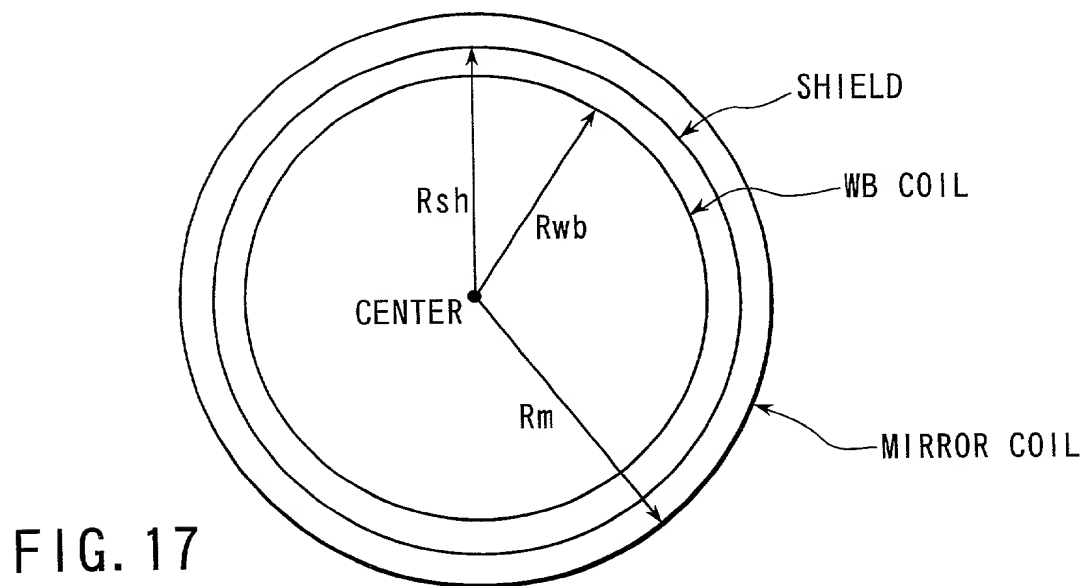
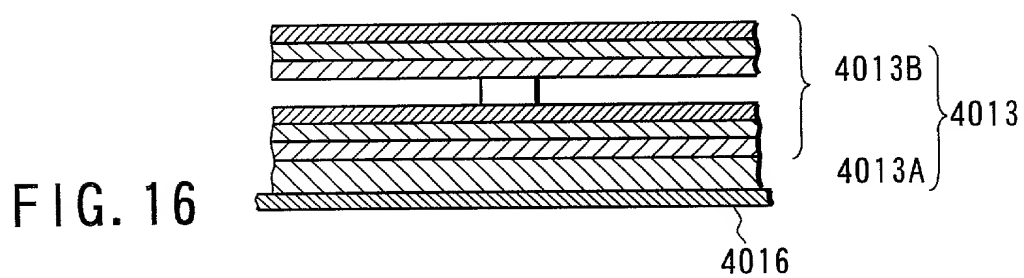
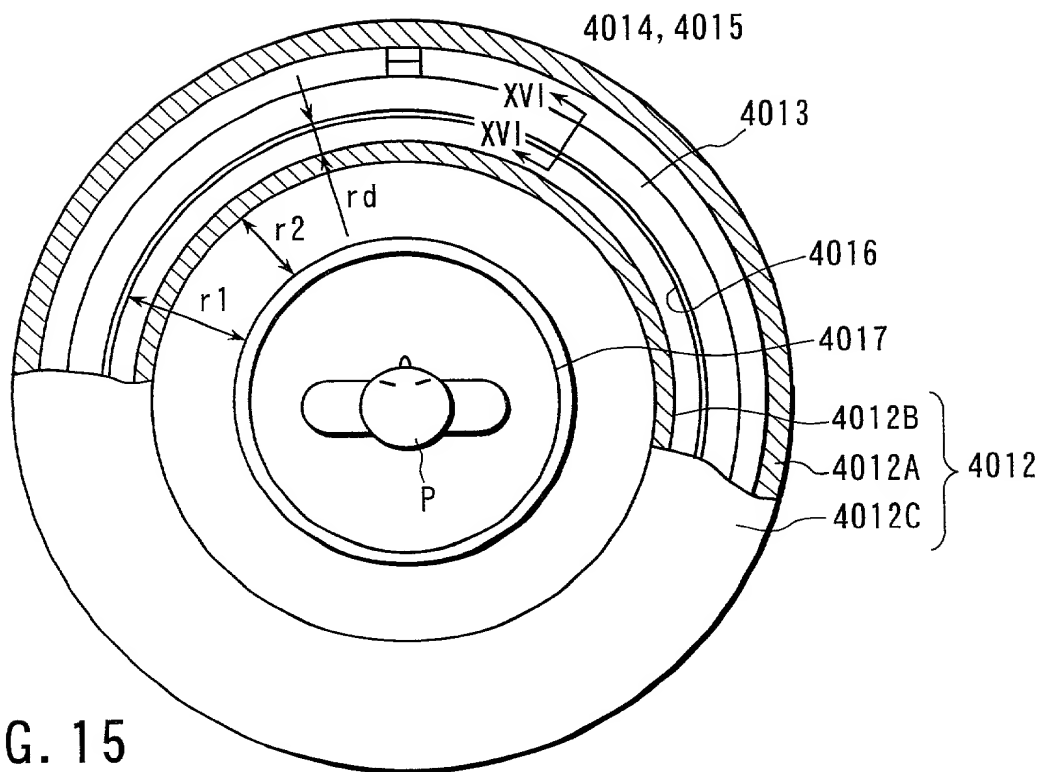


FIG. 14



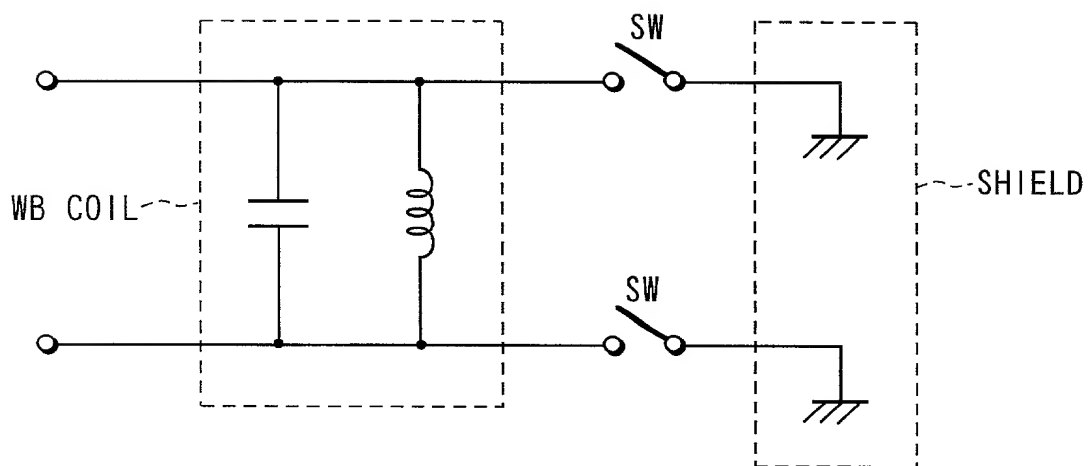


FIG. 18 PRIOR ART

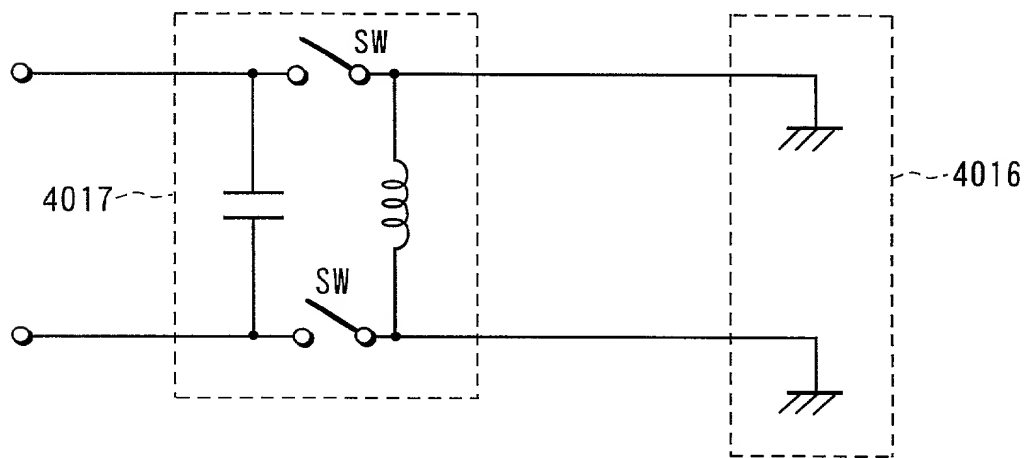
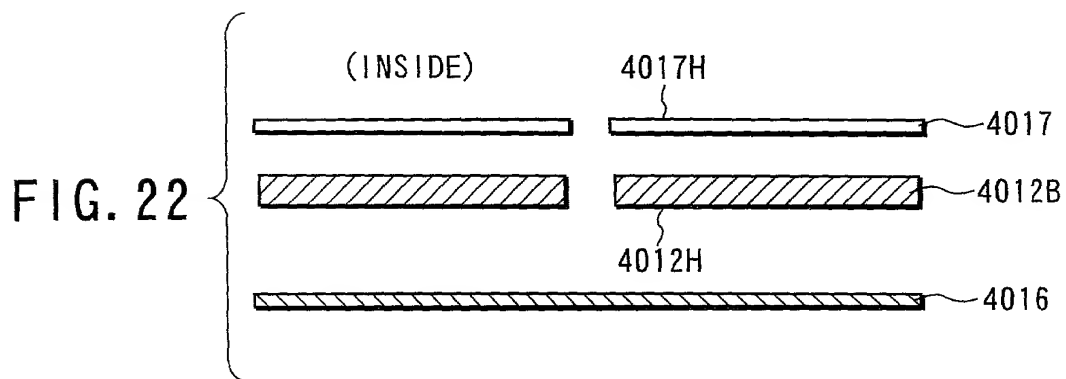
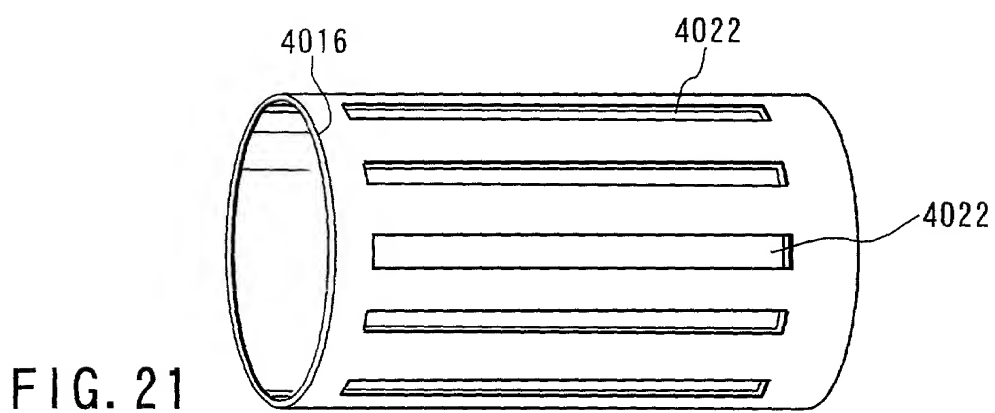
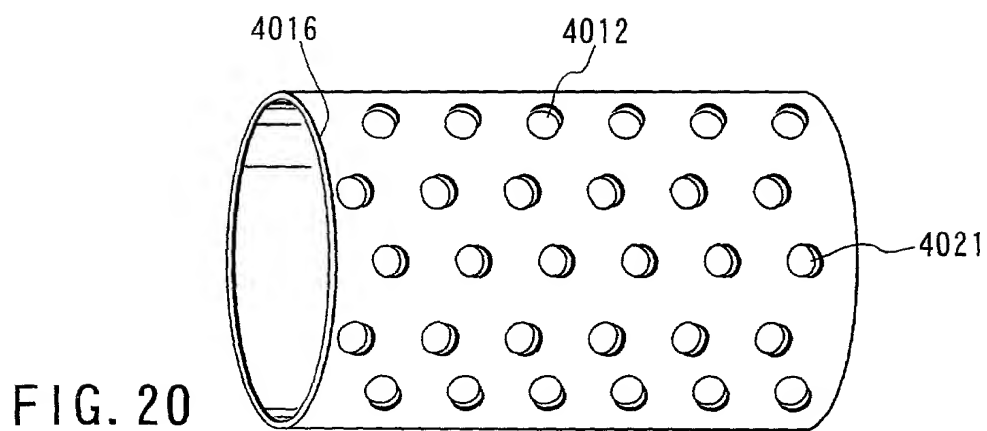


FIG. 19



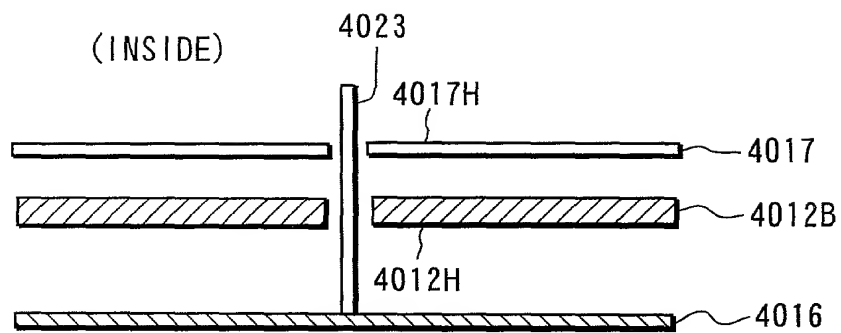


FIG. 23

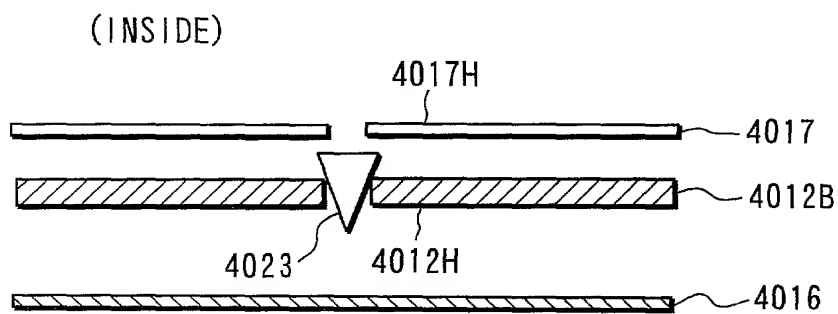


FIG. 24

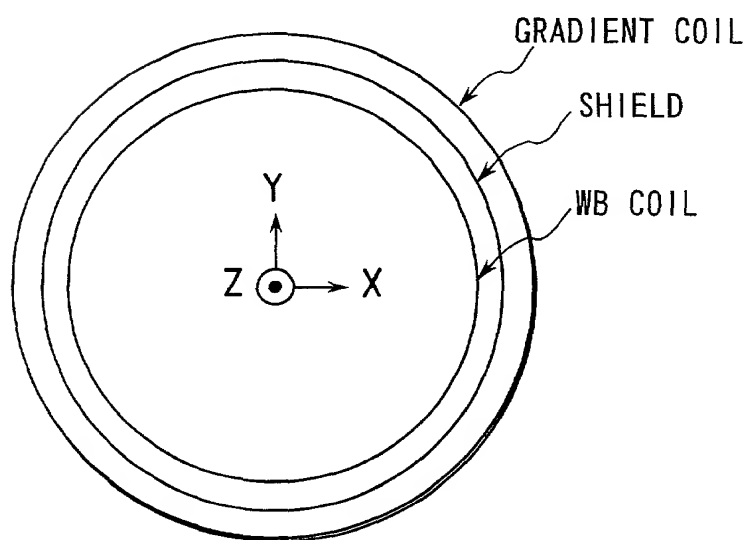


FIG. 25

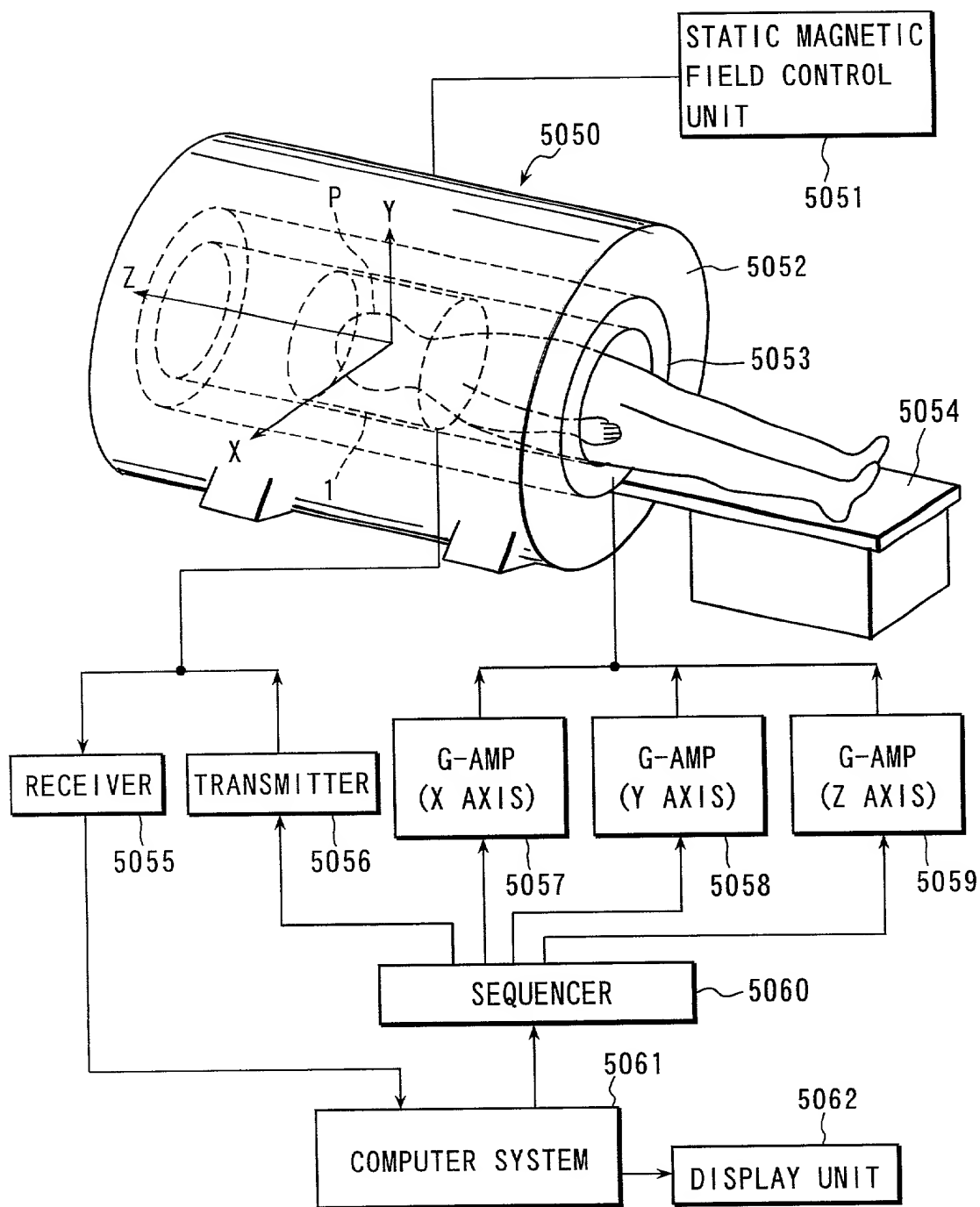


FIG. 26

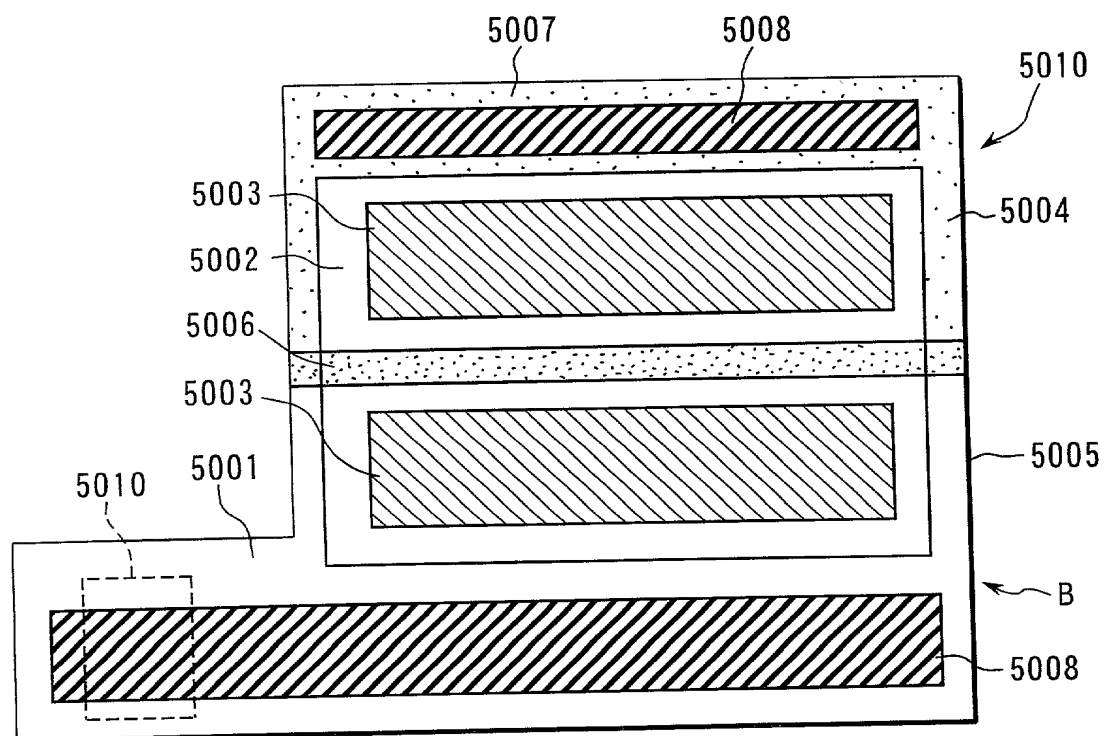
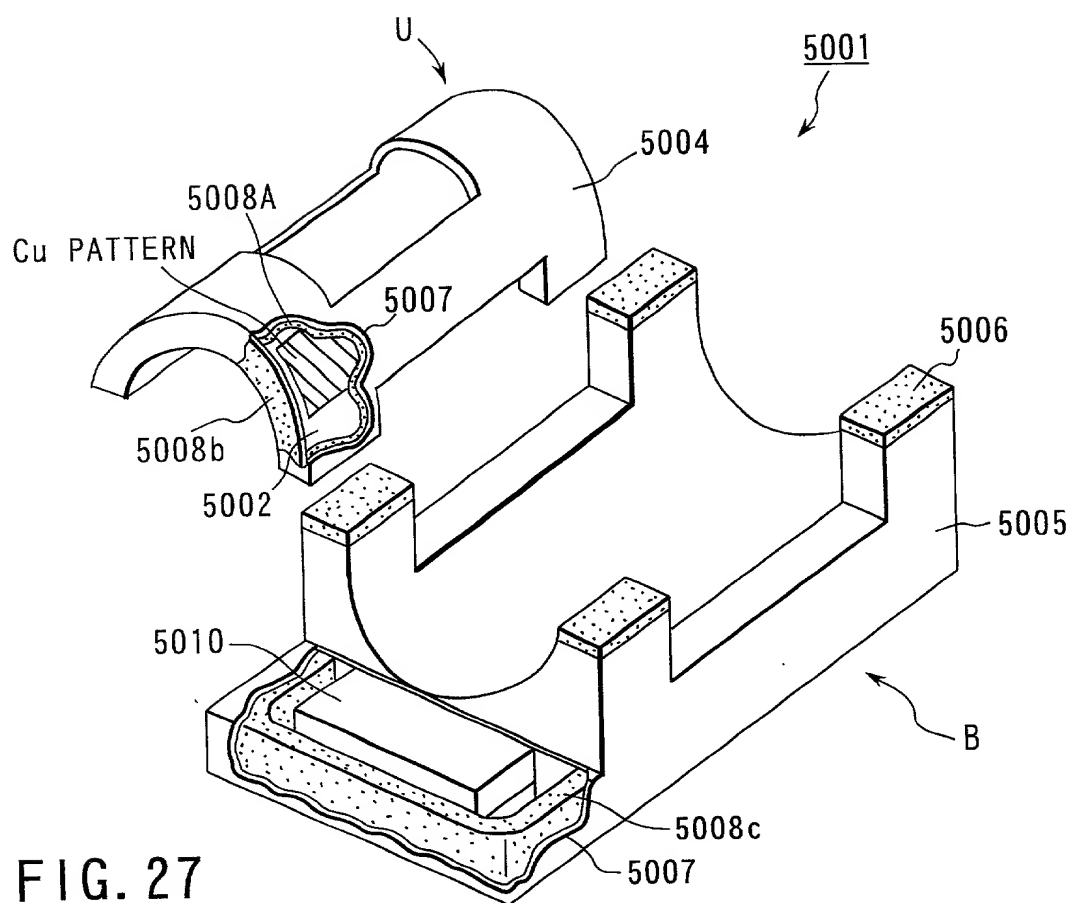


FIG. 29

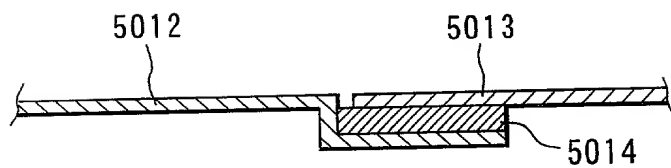
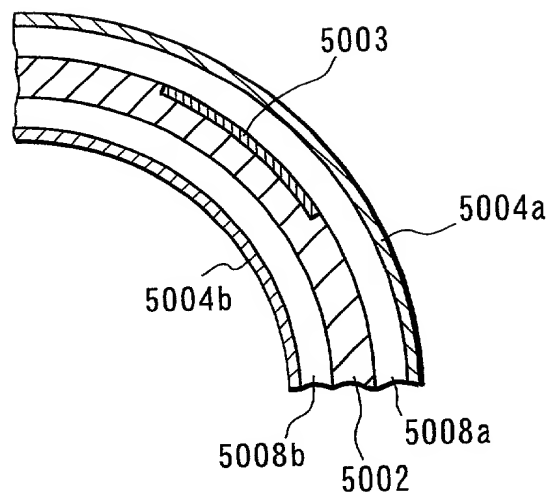


FIG. 30

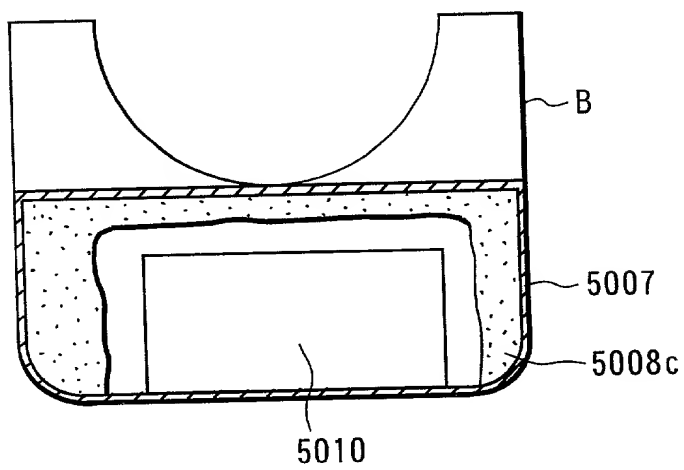


FIG. 31

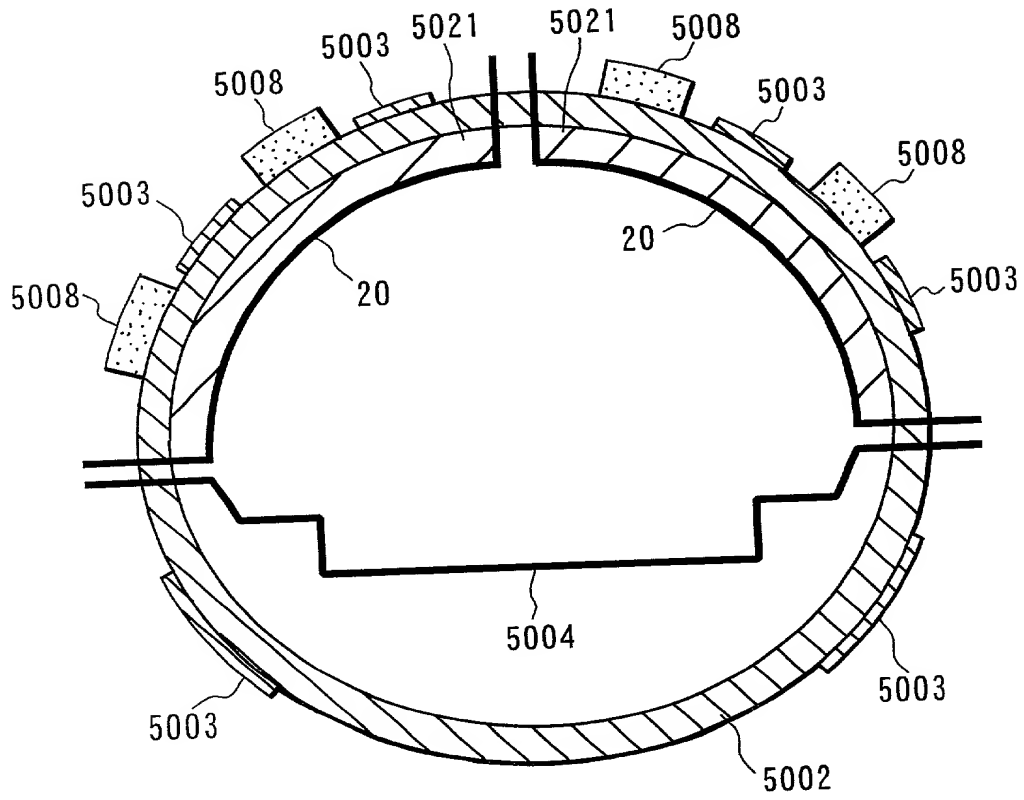


FIG. 32

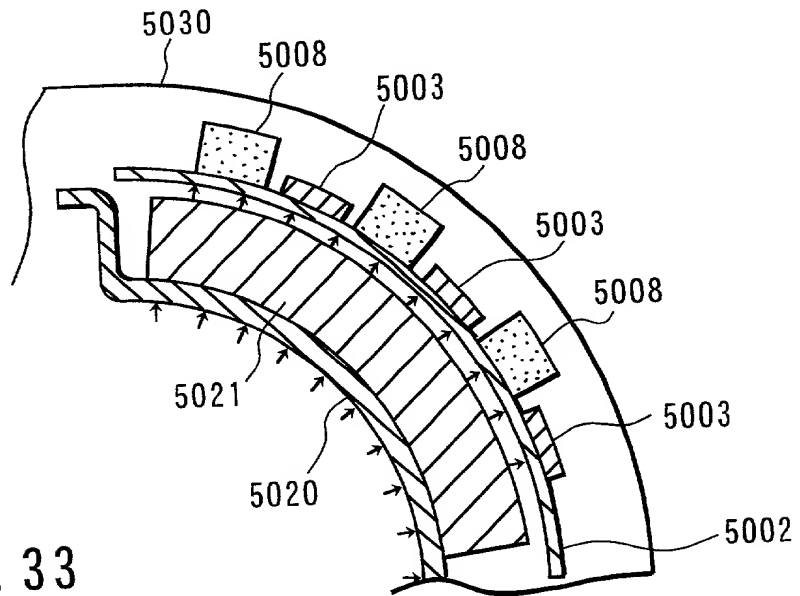


FIG. 33

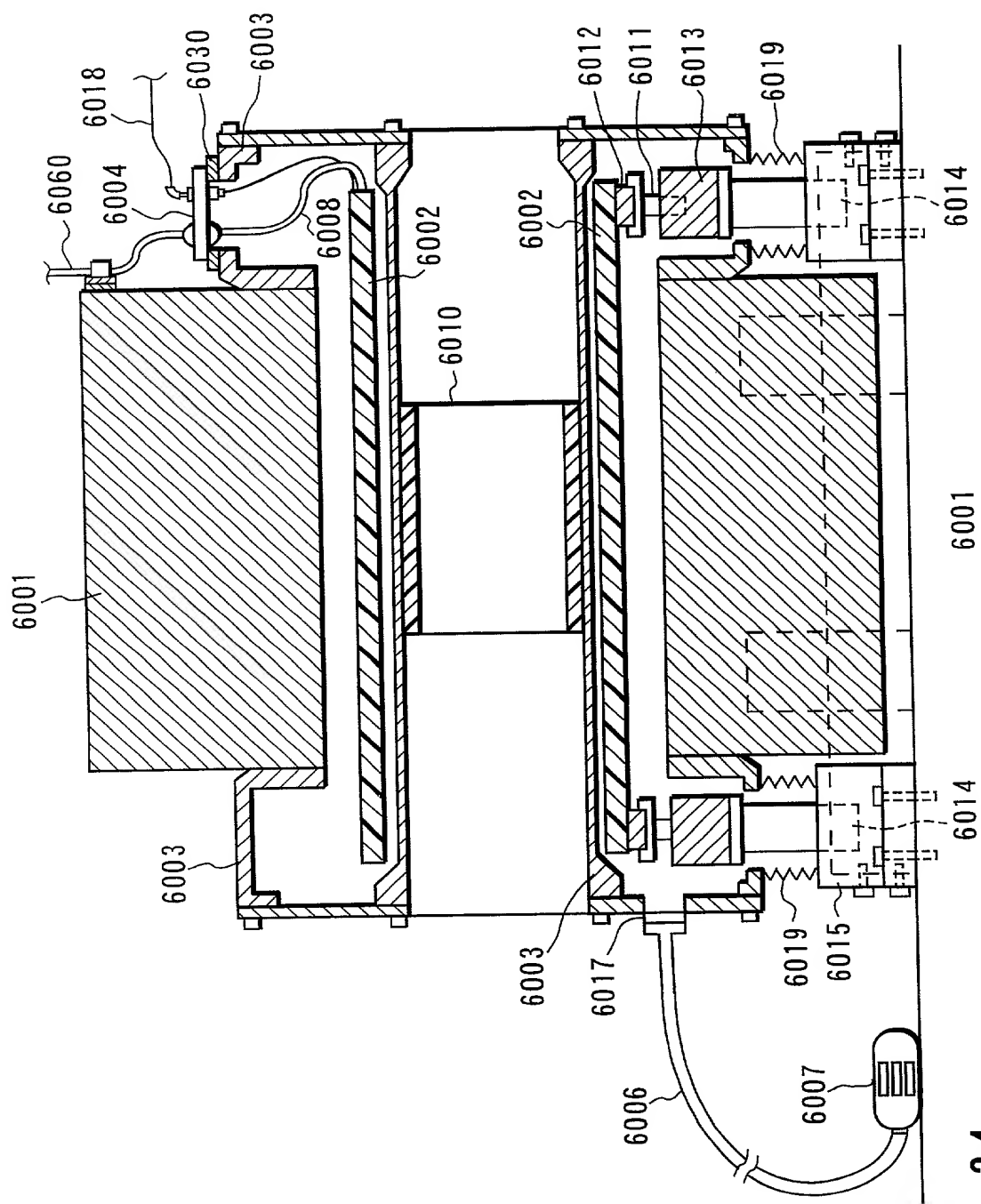
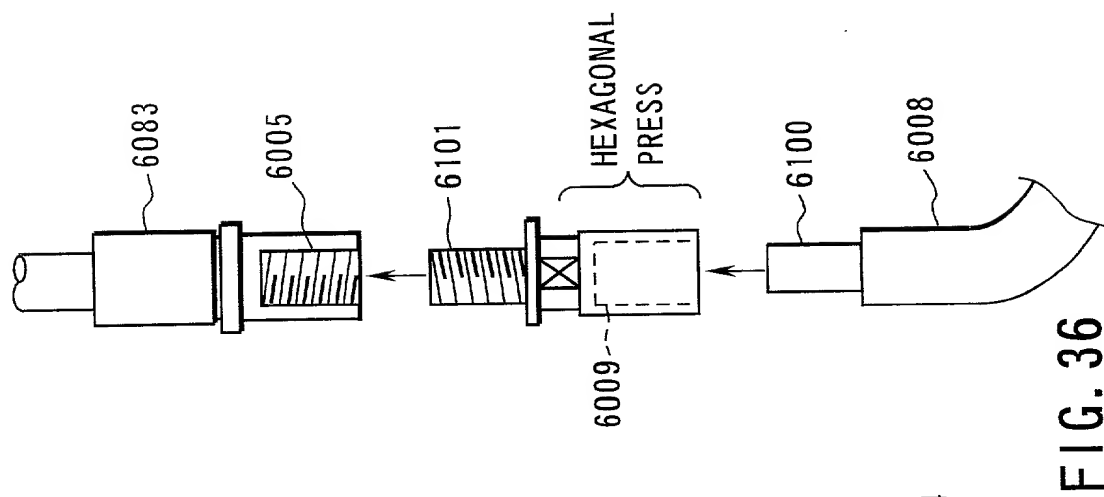
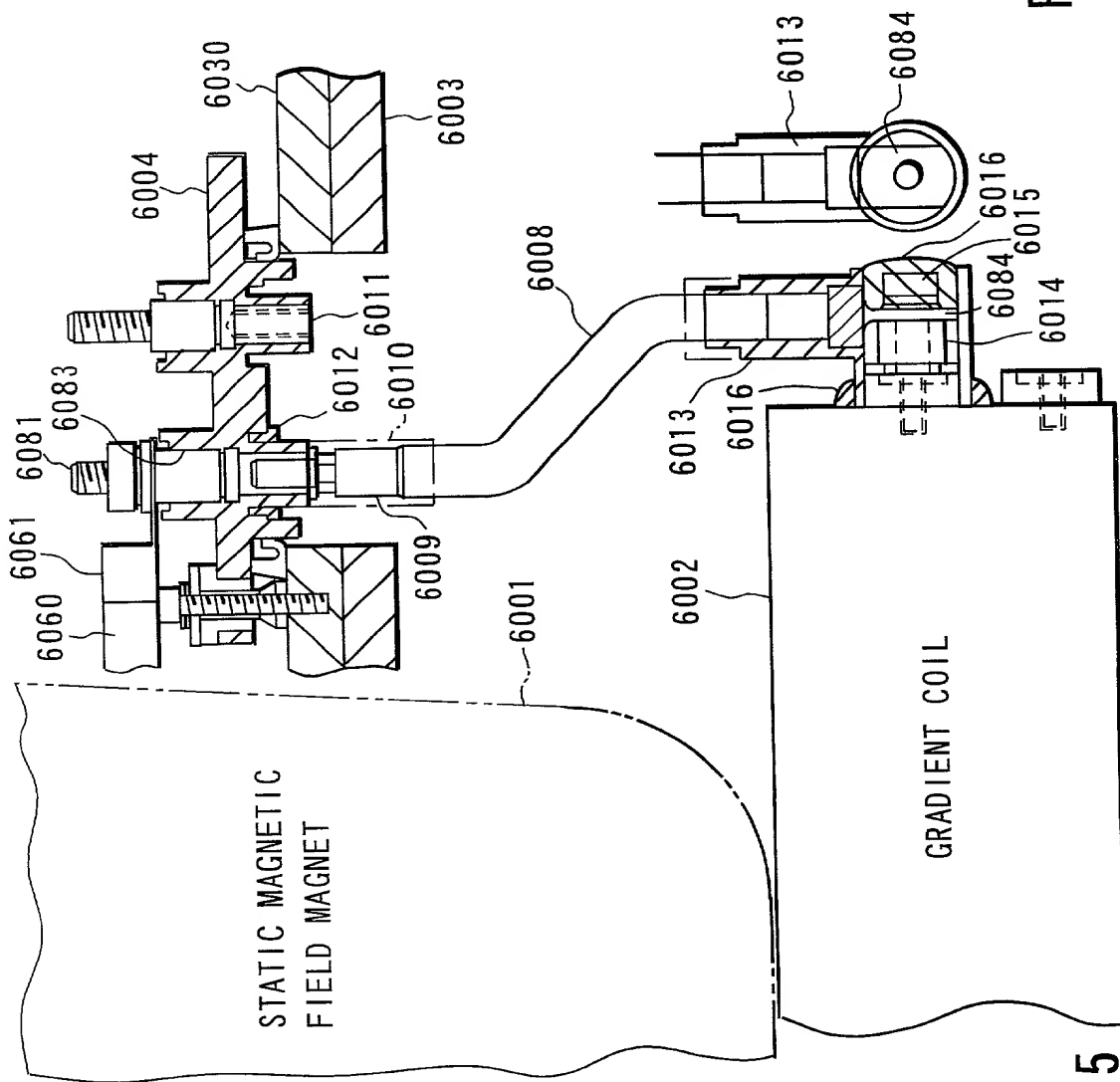


FIG. 34



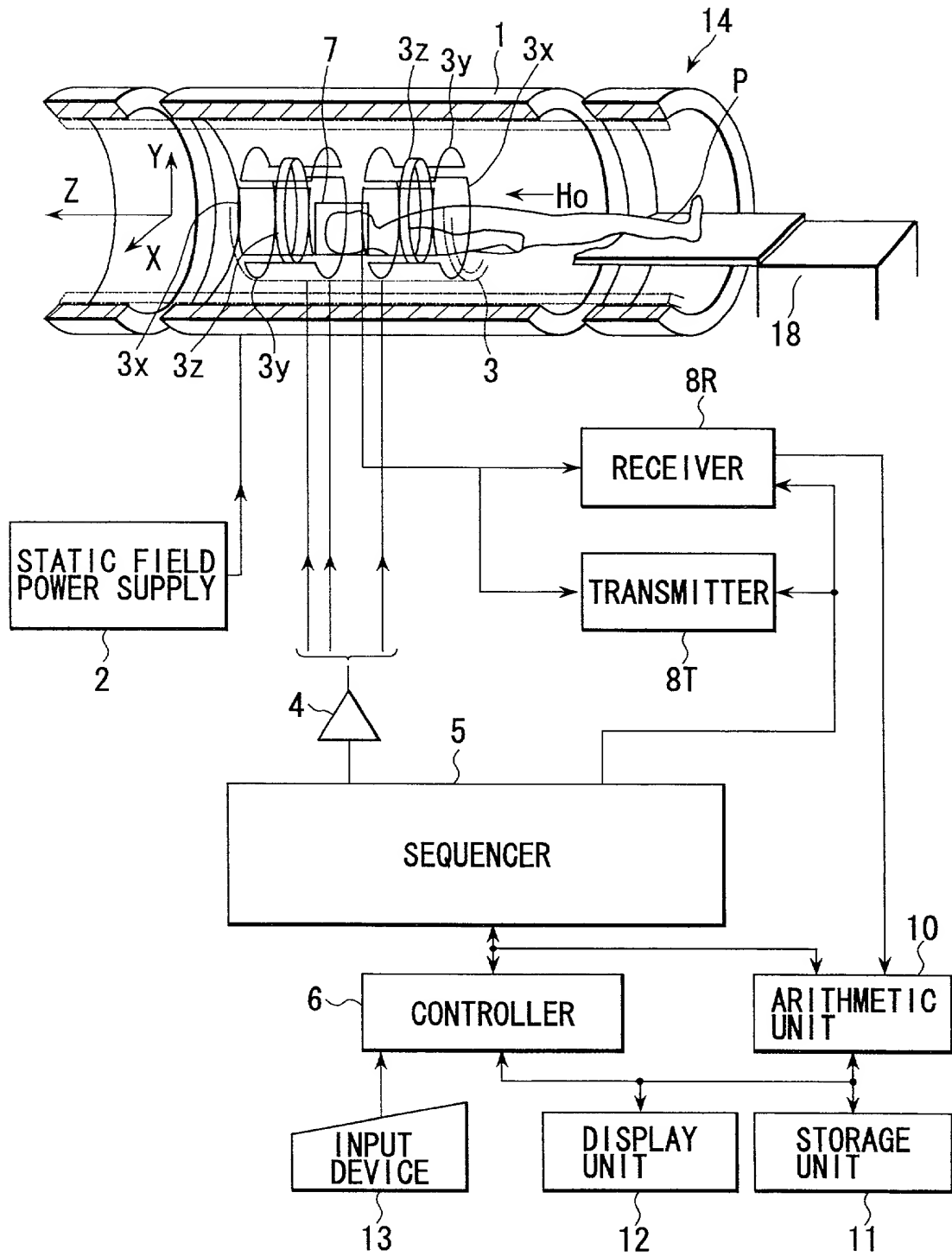


FIG. 37

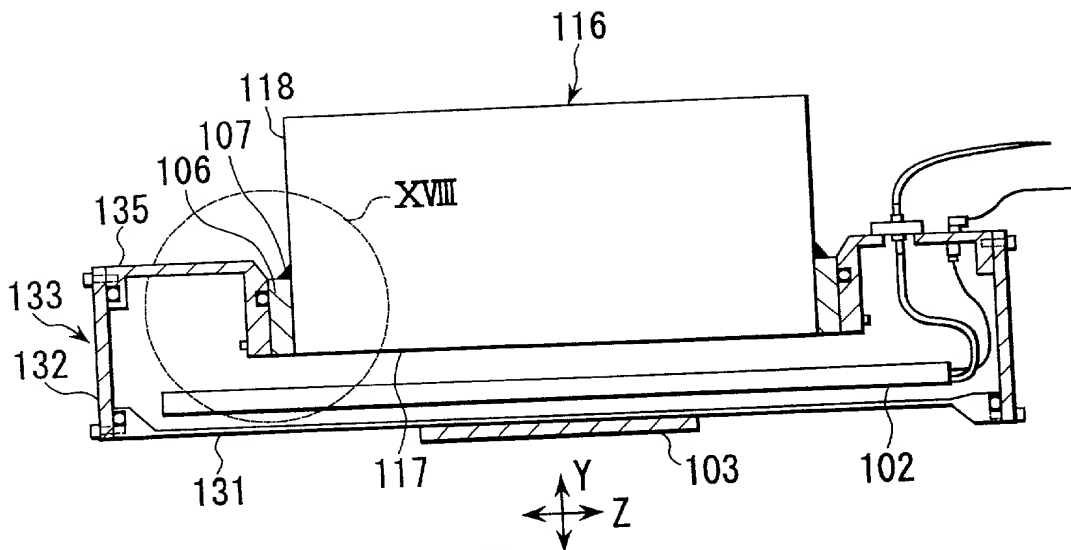


FIG. 38

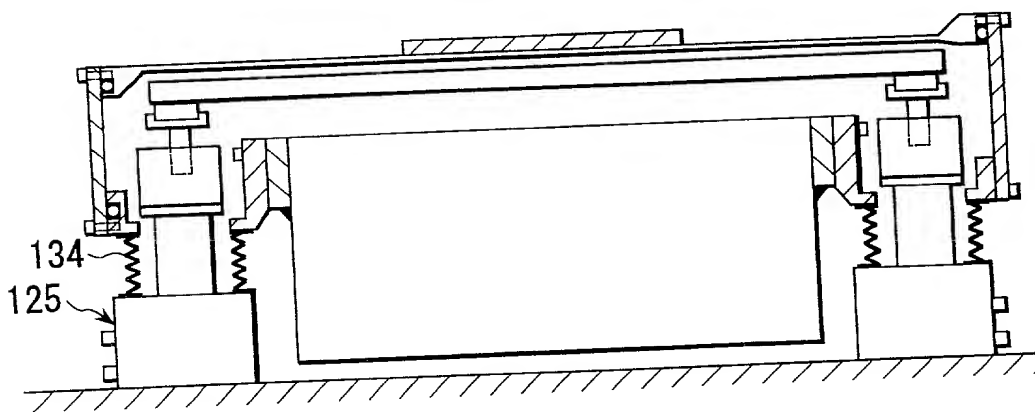
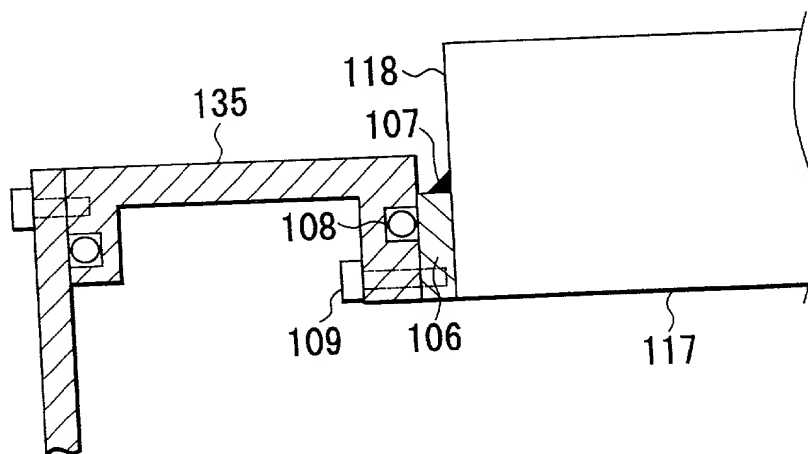
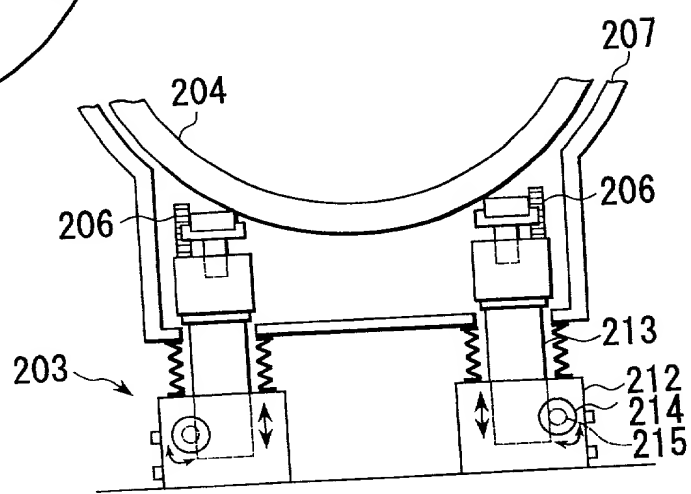
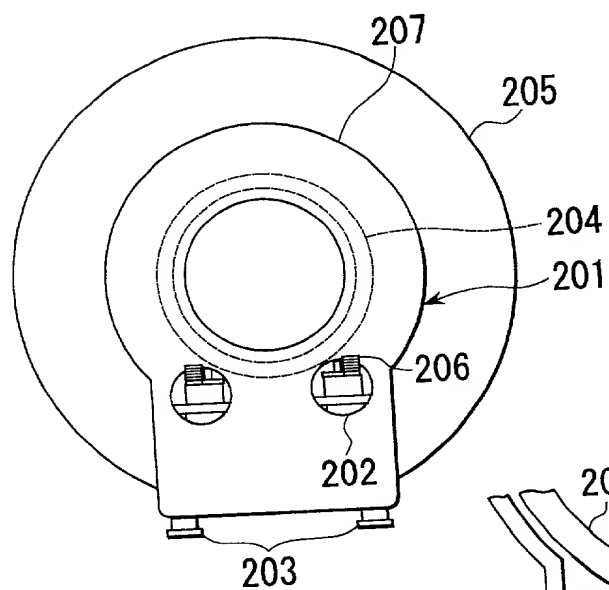
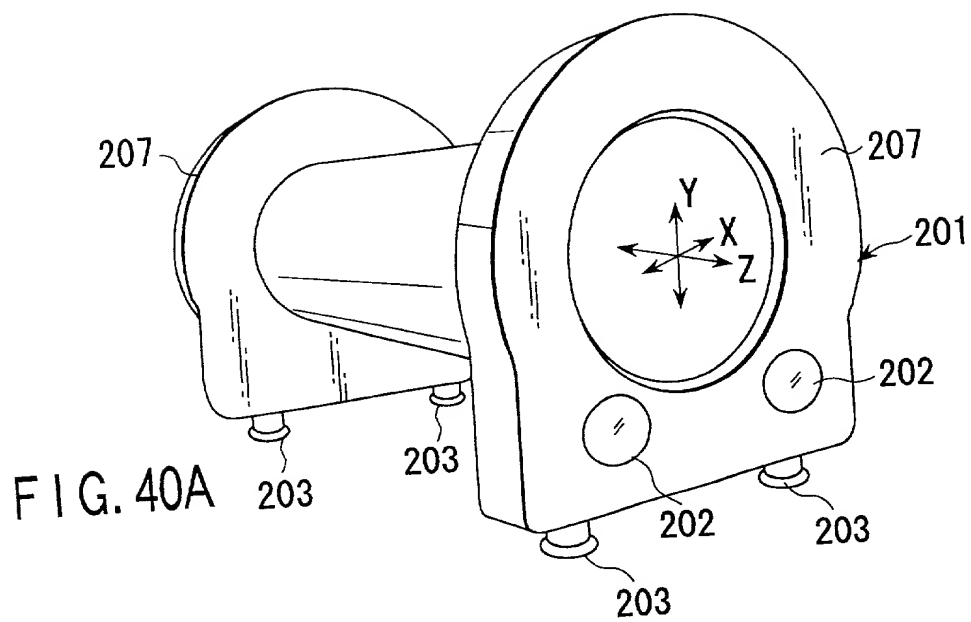


FIG. 39





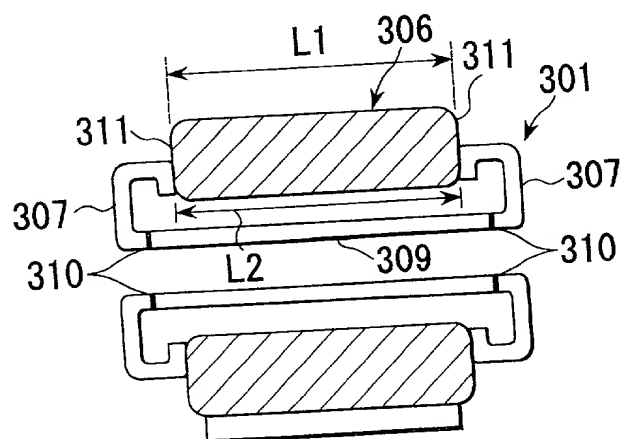
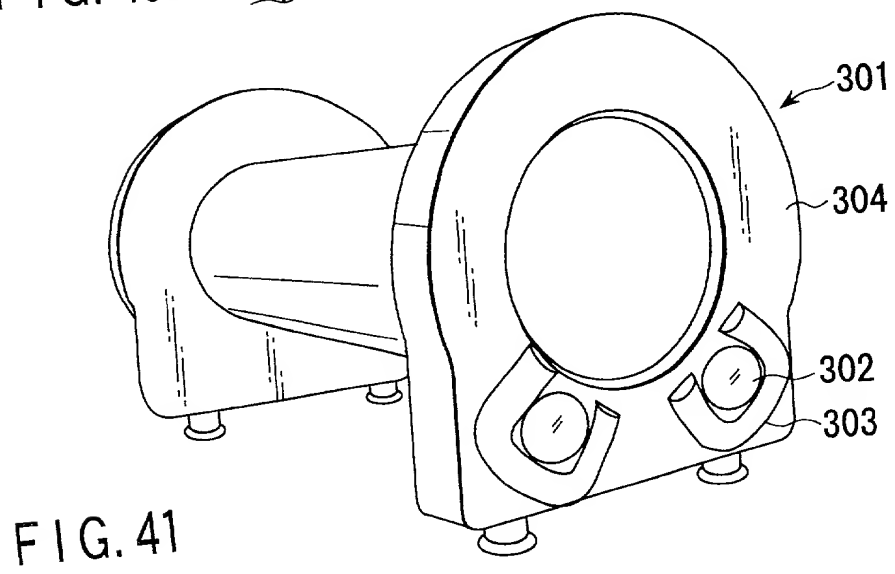
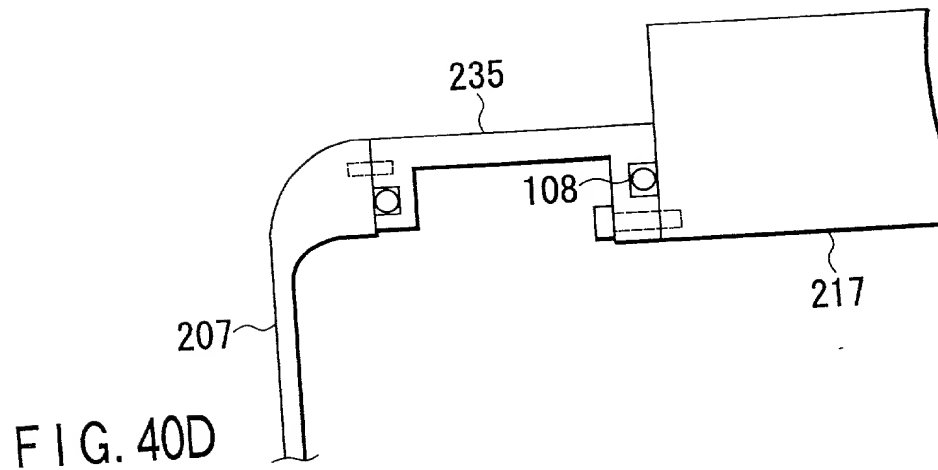
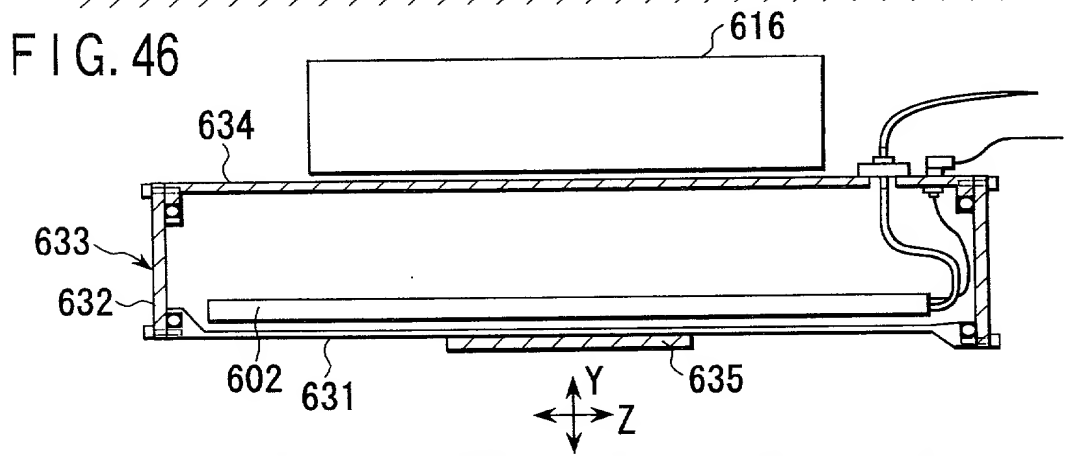
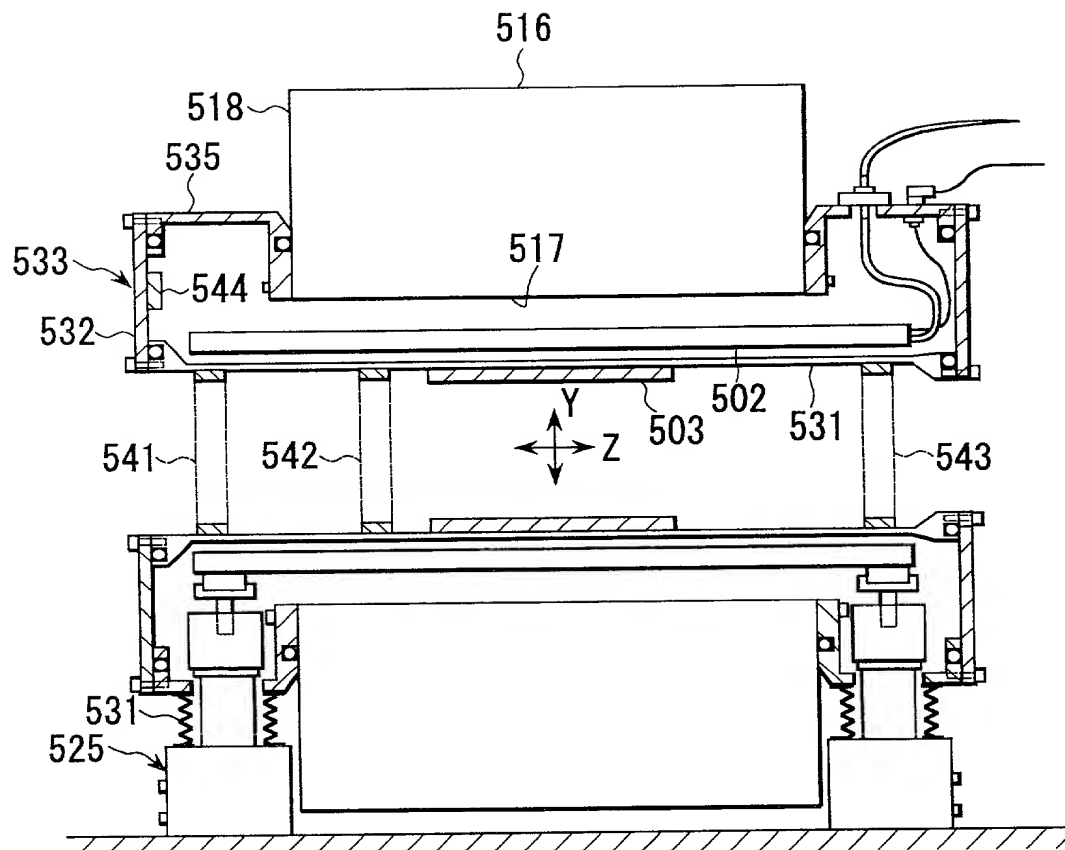


FIG. 45



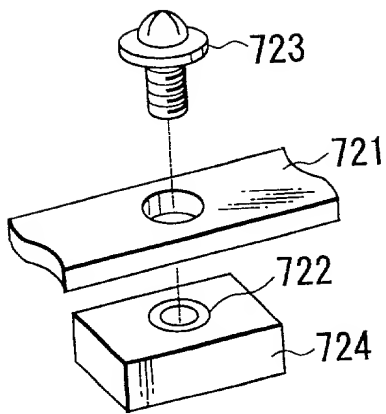


FIG. 48A

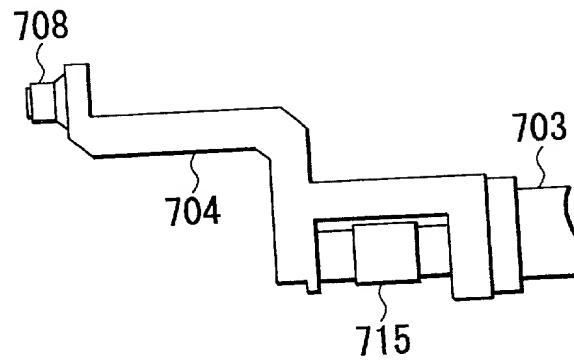


FIG. 49

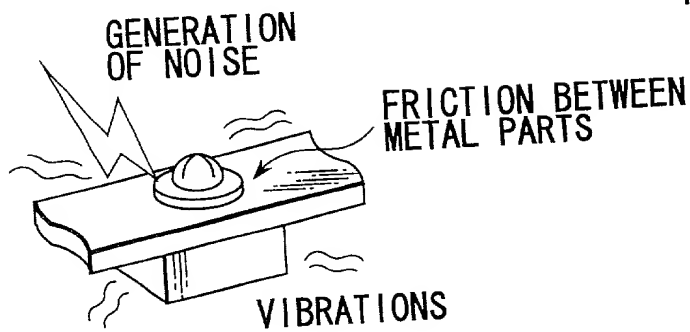


FIG. 48B

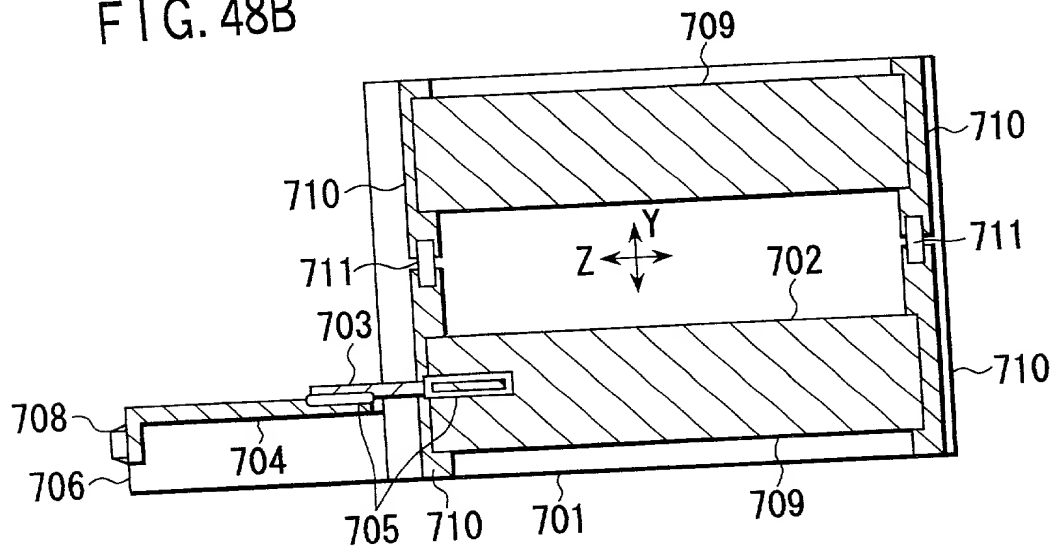


FIG. 50

FIG. 51

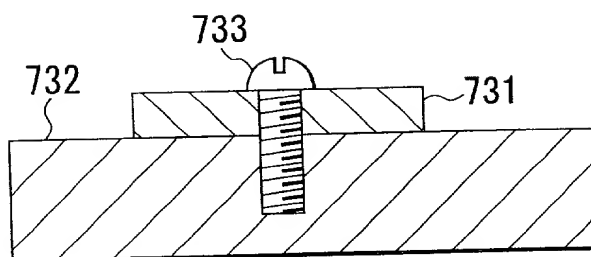


FIG. 52

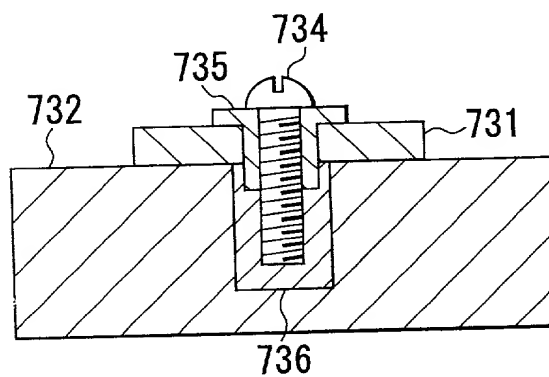


FIG. 53

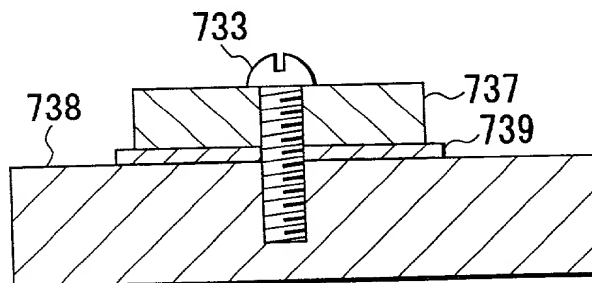


FIG. 54

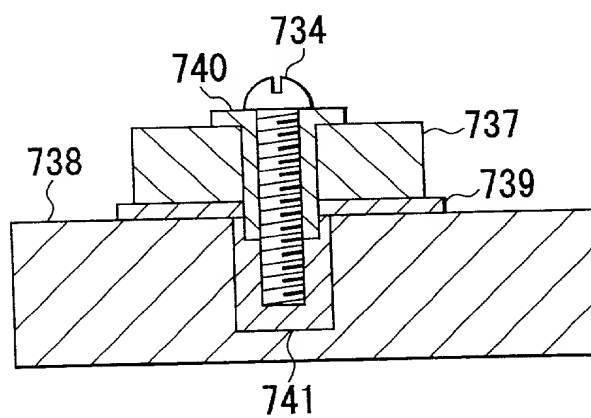


FIG. 55

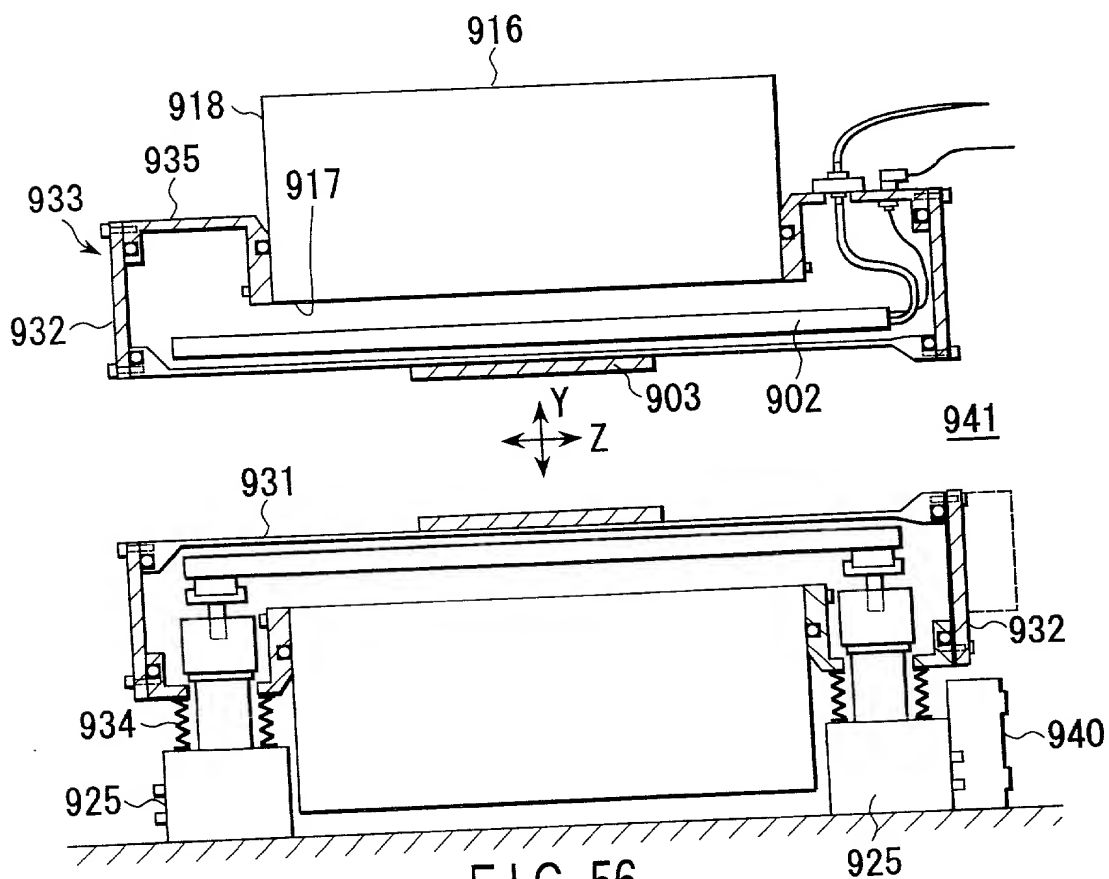
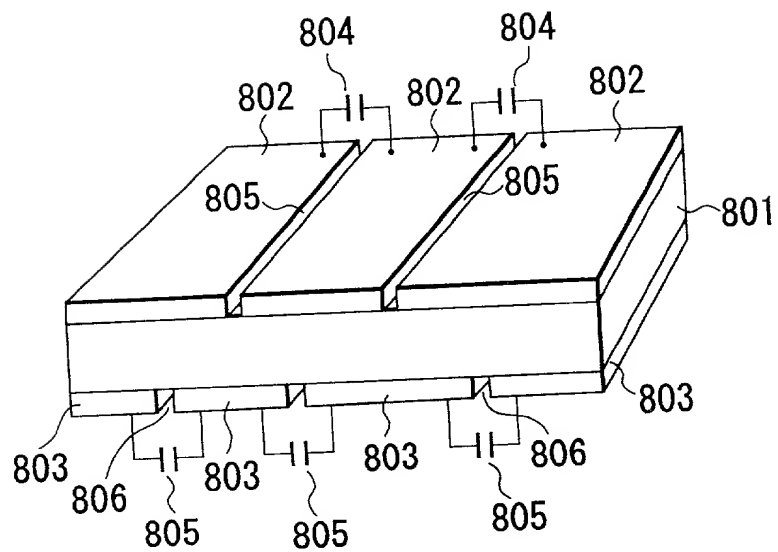


FIG. 56

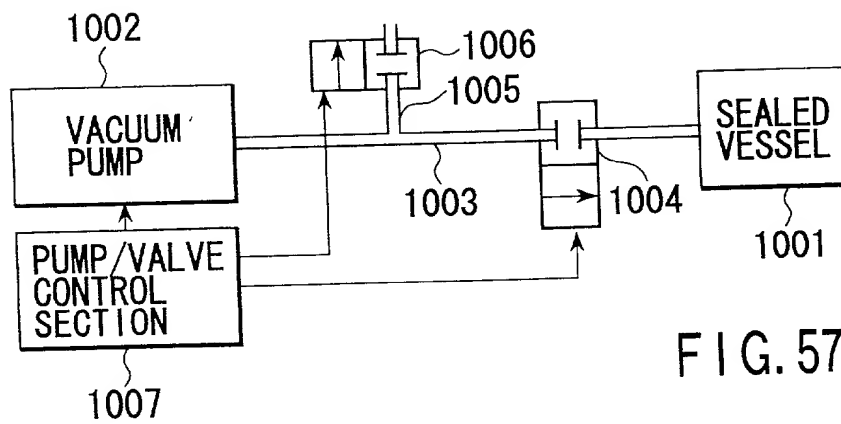


FIG. 57

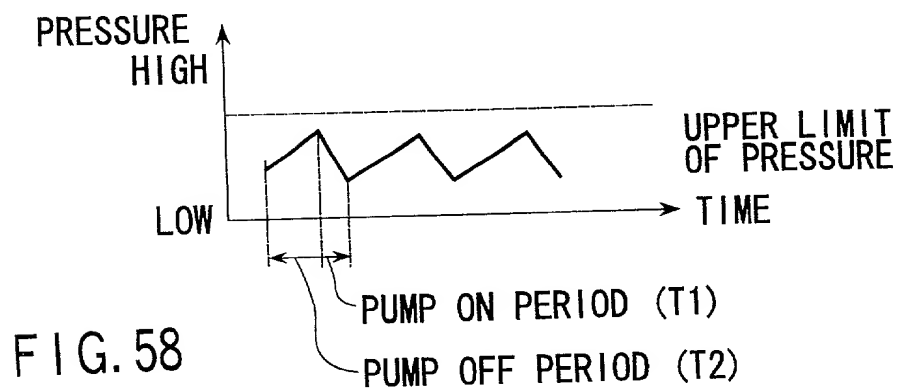


FIG. 58

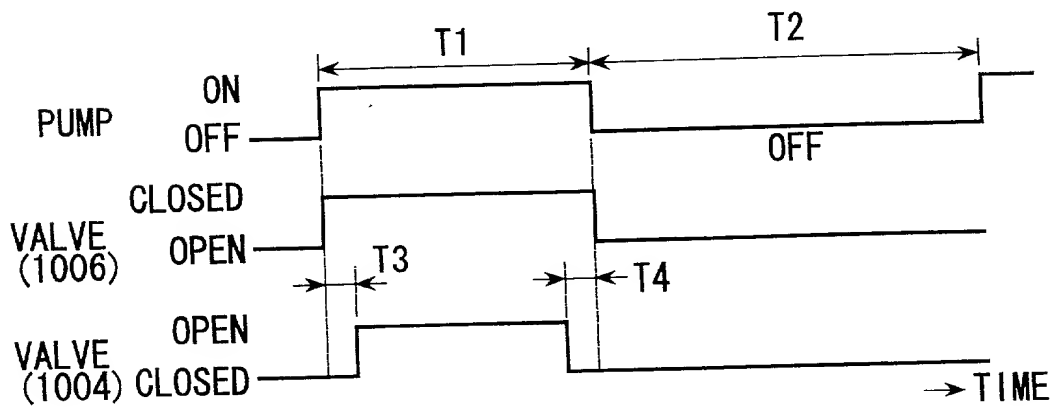


FIG. 59

